PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Arup Bhattacharyya	Examiner: Thomas L. Dickey
Serial No.: 10/612,793	Group Art Unit: 2826
Filed: July 02, 2003	Docket: 1303.111US1

For: HIGH-PERFORMANCE ONE-TRANSISTOR MEMORY CELL

REPLY BRIEF UNDER 37 CFR § 41.41

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Reply Brief is filed in response to the Examiner's Answer (hereinafter "Answer"), mailed on August 7, 2009, and supplements the Appeal Brief filed by the Appellant on May 12, 2009. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 19-0743.

REPLY

Appellant has reviewed the Answer, and believes the statements in the original Appeal Brief remain accurate and compelling. In responding to the Answer, Appellant respectfully maintains that the Appeal Brief, which is hereby incorporated by reference and reasserted in response, overcomes the original grounds of rejection.

This Reply address some comments made by the Office in the Answer.

(5) Summary of Claimed Subject Matter (Pages 2-4 of Answer)

The Office incorrectly states that "Appellant characterizes every independent claim on appeal as including an n/i/p diode that is required to have no gate; however the summary refers to Figures (1B, 2B, 3B, 4B, and 5B) showing n/i/p diodes that have gates."

With respect to Claim 1, for example, Appellant stated that the "diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 230-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23). The phrase "without gating the diode" is not the same as "requiring no gate." "Gating" is an action word. A device is gated by applying an appropriate signal to a gate of the device. If a device has a gate but is not being gated, the signal is not being applied to the gate of the device. A device that does not have a gate also is not gated.

Claim 3 depends on claim 1 and provides the further limitation that the diode is a gate-controlled diode, and that the memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states. The device can switch without gating the diode, as recited in claim 1, but the gating of claim 3 enhances the switching (see also page 3 lines 15-17 of the Specification, which states that various embodiments gate the integrated diode to enhance speed and reduce standby power for the memory cell.).

Appellant does not intend to limit the claimed invention to the un-gated embodiments of figures 1A, 2A, 3A, 4A, 5A, as asserted by the Office in the Answer. The diodes in Figures 1B, 2B, 3B, 4B, and 5B have structures to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode. A pulse does not have

to be applied to the diode gates illustrated in these figures to switch states, although gating the diode (applying the signal to the diode gate) enhances the switching.

The Office refers to Appellant's arguments during prosecution to avoid Baba. Appellant distinguished a "diode" from the "field effect transistor" of Baba, because the field effect transistor (FET) requires a gate voltage to change states (pages 21-24 of the Response dated July 9, 2009).

FIG. 1 of Baba is identified as prior art for Baba, and is further identified as a three terminal device that uses reverse-biased breakdown effects (col. 1 line 38 to col. 3 line 13). FIG. 1 is not a PIN diode. By way of example, region 11 is not an intrinsic region but rather is a doped region (col. 1 lines 40-42). Without an intrinsic region, the device of FIG. 1 cannot be a PIN diode.

Baba FIG. 1

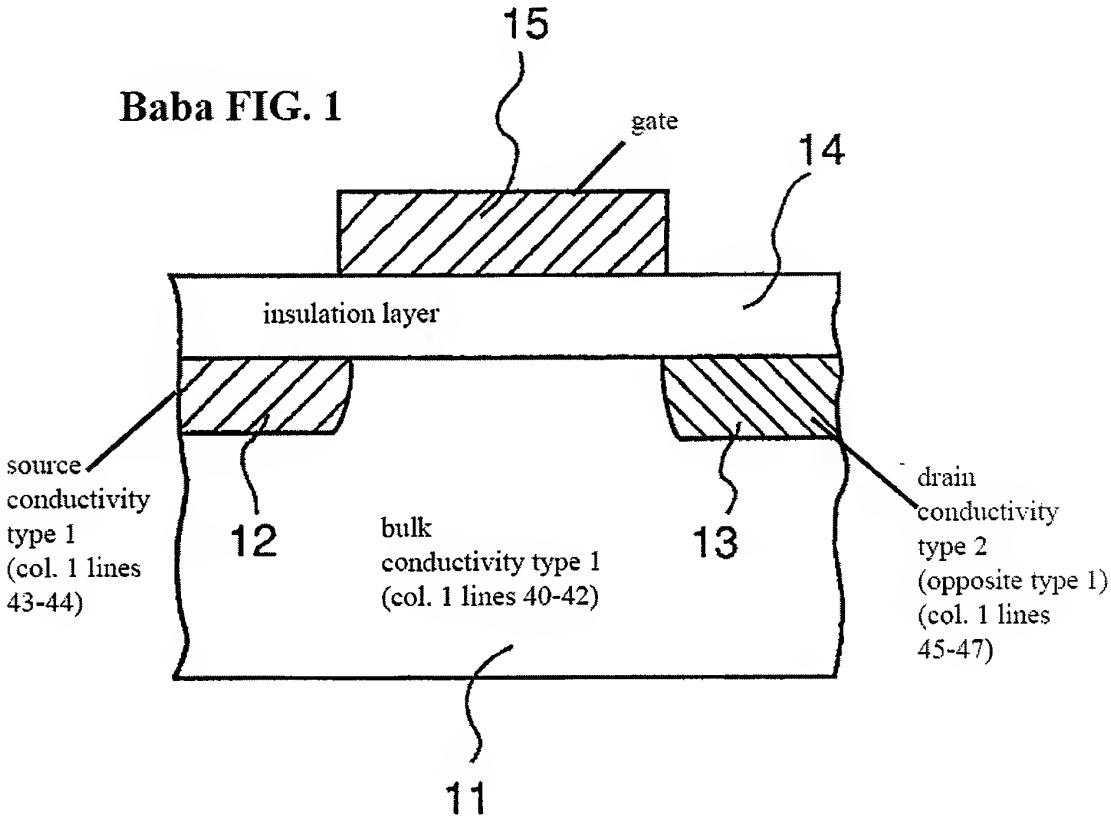
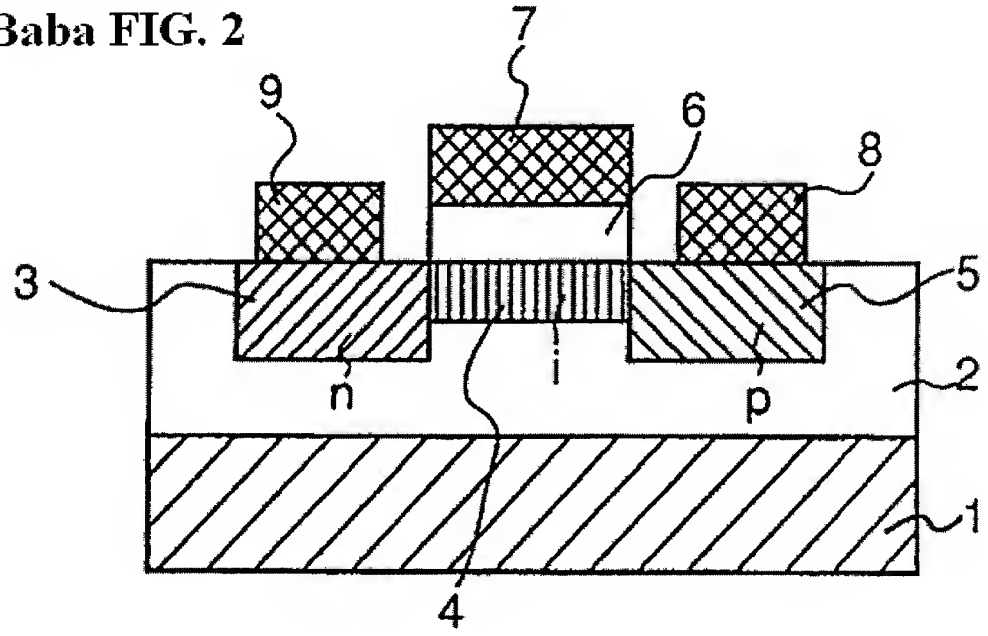
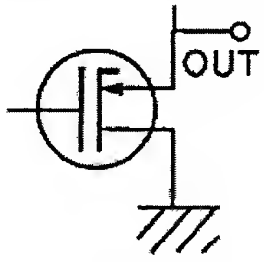


FIG. 2 of Baba is identified as a three terminal tunnel device, and this device is illustrated in FIG. 3 as a field effect transistor (FET).

Baba FIG. 2



Baba FIG. 3



Further, Baba claims its device as a field effect transistor (see claims 1-26 of Baba). In an **enhancement mode**, a voltage needs to be applied to the gate before carriers will tunnel (Baba, col. 3 line 64 to col. 4 line 16), and the amount of tunneling current depends on the gate voltage magnitude (Baba, col. 4 lines 17-22). No tunneling current will occur in the enhancement mode if no voltage or a low voltage is applied to the gate (control electrode) (Baba, col. 4 lines 30-36). In a **depletion mode**, a tunneling current will flow if no voltage is applied to the control electrode (Baba, col. 3 lines 37-45) and the tunneling current is interrupted if a predetermined voltage is applied to the control electrode (Baba, col. 3 lines 46-52). Thus, Baba describes the

operation of field effect tunneling transistors, and indicates that a gate signal ("gating") is required to switch states for either an enhancement mode or depletion mode transistor.

A diode is different than a transistor. A diode gate is not necessary to switch states for the diode.

(9) Grounds of Rejection

On page 17 of the Answer, the Office states: 'The question is, **taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art**, would it have been obvious to achieve the invention of claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71 -74, and 77 **by substituting** the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for Nemati et al.'s negative differential resistance NPNP thyristor device?" (emphasis added by Appellant).

It appears that the only criteria that the Office has for "substitution" is that they are both identified as negative differential devices. However, there are significant differences between resonant tunneling diodes (e.g. very narrow potential barrier to allow tunneling current) forming a latch and a thyristor (e.g. high current). These differences would be recognized by one of ordinary skill in the art -- particularly if as argued by the Office they have an "extremely" high level of skill.

On page 18 of the Answer, the Office states: "Krivokapic discloses that the substituted components and their functions were known in the art." This is a misleading statement. Krivokapic identifies resonant tunneling diodes (RTDs) as exhibiting negative differential resistance. However, Krivokapic does not disclose that RTDs are substitutable for all other negative differential resistance devices.

In contrast to the Office's position, Nemati et al. indicate that there are different NDR devices and that these different NDR devices have different basis for operation such as bipolar transistor and quantum-effect devices (Nemati et al. at col. 3 lines 51 to col. 2 lines 26). Given their different basis of operation, one of ordinary skill in the art would not substitute a bipolar transistor with a quantum-effect device. Similarly, given their different basis of operation, one of ordinary skill in the art would not substitute a resonant tunneling device (Krivokapic) in place

of a thyristor (Nemati et al.). They have different functions and principles of operations, such that one of ordinary skill in the art would not believe they are equivalent and substitutable.

The Office makes the following argument on page 18 of the Answer. "Further, Krivokapic discloses that those of skill in the art were familiar with a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode where tunneling occurs through a potential barrier having a very narrow width, so that the frequency response of a resonant tunneling device is not limited by the diffusion or transit time of charge carriers. Instead, the frequency response is limited only by the circuit capacitance and impedance of the device, generating an improved response over the negative differential resistance NPNP thyristor device used in Nemati et al.'s memory cell. From the similarities between the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode and Nemati et al.'s negative differential resistance NPNP thyristor device, one of skill in the art would have been able to conclude that negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode could have substituted for the negative differential resistance NPNP thyristor device of Nemati et al.'s memory cell." The Office fails to consider the very narrow width of the potential barrier as a difference between an RTD and a thyristor. Further, the Office fails to appreciate that resonant tunneling occurs only if the quantum well thickness and the barrier thickness for an RTD are sufficiently small. If the quantum well thickness and barrier thickness are appropriately small, a set of discrete barrier energy levels exist inside the well, and an incident electrode tunnels through the double barrier with a unity (100%) transmission coefficient when the incident electron has an energy that exactly equal one of the discrete energy levels inside the well.

The Office makes the following argument on page 18 of the Answer. "One of skill in the art would have had reason to predict (based on its functioning in Krivokapic's disclosure) that negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode would have continued functioning in Nemati et al.'s memory cell much as it did in Krivokapic's disclosure and that after the substitution, Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al." The Office neither identified nor appreciated how the resonant tunneling diode functions in Krivokapic. Also, the Office never

clearly described how the device of Krivokapic would be substituted into the device of Nemati et al. Krivokapic describes an RTD latch. The latch includes two RTDs in series. The Office did not indicate if one RTD was being substituted for the thyristor, or if the latch was being substituted for the thyristor. Further, the Office replaces a high current device (thyristor) with at least one a tunneling current device (an RTD or RTD latch). The Office never addresses what would need to be changed in the Nemati et al. device to accommodate a tunneling current device with a very narrow potential barrier. For example, what voltage could be placed across the RTD latch. Additionally, the Office fails to consider the amount of charge that should be stored on the storage node 24 of Nemati et al. in order for the storage state to be read or the amount of voltage that Nemati et al. places on the storage node (0.4 to 0.5V) (Nemati et al, col. 6 line 42). Further, the resonant tunneling current is a small current (either to or from the storage node) that would make any change in memory state (charging or discharging the storage node) in the memory of Nemati et al. very slow. Nemati et al. indicate that the switching speed should be fast (e.g. Nemati et al., col. 2 lines 9-10; col. 3 lines 56-65, col. 4 lines 5-6). One of ordinary skill in the art would understand that this is not a "simple substitution" because of the differences between an RTD and a thyristor.

(10) Response to Arguments

On page 20 of the Answer, the Office asserts that Nemati discloses an embodiment that include a bipolar transistor functioning as an NDR device and an embodiments that includes a quantum-effect device operating as an NDR device.

One of ordinary skill in the art would not believe that one type of NDR devices is substitutable with any other NDR device. Nemati et al. clearly indicate, in the background section, that there is a "variety" of NDR devices, and that these different NDR devices have different basis of operation. Appellant identified this portion of Nemati et al. to support Appellant's contention that one of ordinary skill in the art would not substitute a resonant tunneling device (quantum-effect) for a thyristor. One of ordinary skill in the art appreciates the differences in the basis of operation and appreciates that the device of Nemati would not work if an RTD latch (two devices) or a single RTD device was substituted for a thyristor. For example,

the RTD has a very narrow potential barrier to allow tunneling due to the small quantum well thickness and barrier thickness.

With reference to page 24 of the Answer, Appellant does not disagree with the MPEP by arguing that substitution cannot be used, in general, to combine references. However, Applicant disagrees with the Office's reliance on "simple substitution" to substitute an RTD for a thyristor. With reference to **MPEP 2144.01**, Applicant respectfully asserts:

- To rely on substitution, **the equivalency must be recognized in the art**. As provided above, one of ordinary skill in the art would not believe that the RTD is equivalent to a thyristor. Equivalency requires more than the fact that they are both identified as negative differential devices. Thus, the proposed modification is improper.
- To rely on substitution, **there can be no change in the respective functions**. Because of the different principles of operation, there would have to be a change in their respective functions. Thus, the proposed modification is improper.
- If the Nemati et al. device is modified to include an RTD of Krivokapic, **such a modification would make the Nemati et al. device unsatisfactory for its intended purpose**. For example, if Nemati et al. indicate that switching speed (the time to charge or discharge the storage node) is important, Nemati et al. would find it unsatisfactory to rely on tunneling current to charge or discharge the storage node. Thus, the proposed modification is improper.
- **The proposed modification of the memory cell in Nemati et al. would improperly change the principle of operation of the memory cell.** Thus, the proposed modification is improper.

Appellant notes that the mere statement that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness. It is improper for the Office to only rely on the "negative differential" description of these devices, ignoring the other characteristics of these devices that make them very different devices, and make a conclusory statement that one of ordinary skill in the art could substitute these devices.

On page 26, the Office argues that Appellant's assertion that Nemati's memory device is a "high current density thyristor" is not supported by the evidence of record. The Office points to two embodiments: 1) the array of memory cells, and 2) the power switch structure.
Appellant disagrees with the Offices position, noting that in col. 2 lines 3-6 of Nemati et al. (the background section), Nemati et al. identify problems with using NDR devices in SRAM cells, including large current needed in one or both the stable states of the cell.
Appellant respectfully notes that the power switch structure illustrated in FIG. 8 uses three thyristors (40a, 40b, 40c) to provide more current than a single thyristor (FIG. 1), and further notes that each of the thyristors is constructed in a manner similar to the structure of FIG. 1 (Nemati et al., col. 7 lines 2-4). Thus, the structure with multiple thyristors in FIG. 8 provides more current than the single thyristor in FIG. 1. Even so, the single thyristor used for the memory device has a much higher current density than tunneling current through a resonant tunneling diode.

Conclusion

The pending claims subject to this appeal are believed patentable. Appellant respectfully submits the claims are in condition for allowance and requests the Board issue an order to withdraw the rejection.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402

Date 10-6-09 By _____
Marvin L. Beekman
Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 7th day of October, 2009.

Name Amy Moriarty

Signature _____